REMARKS

The Office action has been carefully considered. Claims 12-15 were allowed. Claim 10 was objected to as being dependent on a rejected base claim (independent claim 8), but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claims 1-9 were rejected under 35 U.S.C. § 102(b) as being anticipated by Bourke et al., U.S. Patent No. 5,509,124 (hereinafter "Bourke").

Applicants thank the Examiner for indicating that the subject matter recited in claims 12-15 is allowable. By present amendment, the specification has been amended and claims 22-31 have been added. Applicants submit that the claims 1-9 as initially presented were in acceptable form. Independent claim 1 has been amended to more particularly point out and claim the subject matter of the invention. Claim 10 has been cancelled and independent claim 8 has been amended to include all the limitations of claim 10 as instructed by the Office action for expediting allowance of claims 8-9. The claims have been amended for clarification and not in view of the prior art and/or for purposes related to patentability. Applicants submit that the claims as filed were patentable over the prior art of record, and that the amendments herein are for purposes of clarifying the claims and/or for expediting allowance of the claims, and not for reasons related to patentability. Reconsideration is respectfully requested.

Turning to the 35 U.S.C. § 102(b) rejections, the present invention generally relates to preserving the state of computer systems when the computer is shut down. Briefly, the present invention provides an improved hibernation method and system, including the use of a modified DMA (Direct Memory Access) mode of transferring data to (and from) the

disk. The modified DMA mode increases data transfer speed, while also freeing the system processor to perform other tasks, including compressing the data to reduce the size of the data that needs to be transferred to (and later from) the disk. For data that is compressed, the present invention also provides an improved decompression mechanism that speeds resume time.

The use of modified DMA for transferring data to and from disk is significantly faster than programmed input/output (PIO), and also frees the processor to perform other tasks while the hard disk controller transfers the data to and from the disk. To accomplish hibernation with DMA while not changing the contents of the memory that are to be preserved, the present invention uses a special, modified DMA engine (including an asynchronous polling I/O protocol) that works by, among other things, polling a hard disk controller status register instead of relying on interrupts to signal the completed status. Between polling cycles, the compression or decompression tasks are performed by the processor. Moreover, the hibernation engine is able to use system software services (e.g., drivers)

To this end, memory devoted for internal driver data structures is allocated in a hibernation-safe memory location or locations, I/O buffer locations are moved into the safe memory range, buffer alignment is controlled, and large I/O requests are split into sequences of smaller ones. More particularly, the hibernation engine communicates with the hard disk controller driver and DMA driver to obtain the hardware and software requirements, e.g., including, what is the largest size I/O request that the hardware handles, the amount of memory needed for the driver's internal structures, the region of memory where an I/O buffer should be located, and what the I/O buffer alignment should be. In this manner, the

drivers do not access memory outside of that reserved for hibernation, and data integrity is preserved.

Bourke on the other hand, does not deal with disabling interrupts on a computer system for entering a state of hibernation. Bourke does not deal with preparing a set of data for writing a set of content of volatile memory to a disk. Nor does Bourke deal with instructing a controller to write the aforementioned data asynchronously to the disk. Rather, Bourke is directed to utilizing programmed input/output (I/O) to operate a computer system. Bourke, abstract. Furthermore, Bourke, as contended in the Office action, is specifically directed to utilizing programmed input/output (I/O) to disable interrupts and prepare data (see col. 38, lines 22-33, col. 40, 48-50), instruct a controller to write data asynchronously to a disk (see col. 22, lines 35-52, col. 40, lines 50-59), polling, in intermittent polling operations, a status register to determine when the write to the disk is complete (see col. 41, lines 14-37, col. 42, lines 42-50), while between polling operations, preparing a second set of data for writing (see col. 42, line 60-col. 43, line 33). Office action pg. 2, sec. 3.

Significantly, Bourke does not disclose or suggest the use of disabling interrupts on a computer system for entering a state of hibernation as recited by applicants. Nor does Bourke disclose or suggest the use of writing a first set of content of volatile memory to a disk as is also recited by applicants. Rather, Bourke states, "[h]owever, the clocking arrangement of the adapter bus is inherently faster, in operation, than the handshaking arrangement of the SPD bus. Therefore, a need exists for an input output interface controller (IOIC), interconnecting the adapter bus to the SPD bus, to act as a buffer between the adapter bus and the SPD bus so that the faster adapter bus will not overrun the slower

SPD bus. The IOIC must therefore comprise a registers and buffers section for storing commands, instructions, and data, an adapter bus control logic for retrieving the commands, instructions and data from the adapter bus for placement in the registers and buffers section of the IOIC and an SPD bus control logic for retrieval of the commands, instructions and data from the register and buffers section of the IOIC for placement on the SPD bus (and vice versa)." Bourke, col. 2, lines 8-22.

Indeed, if anything, Bourke *teaches away* from the use of disabling interrupts on a computer system for entering a state of hibernation as Bourke intends synchronized data transfer during normal operation. Bourke further teaches away from the use of writing a first set of content of volatile memory to a disk as Bourke intends the use of the IOIC to function as a buffer between the faster synchronous bus and the slower asynchronous bus. The use of disabling interrupts on a computer system for entering a state of hibernation is far different from using synchronized data transfer during normal operation. Additionally, the use of writing a first set of content of volatile memory to a disk is far different from the use of the IOIC to function as a buffer between the faster synchronous bus and the slower asynchronous bus.

Anticipation under 35 U.S.C. § 102 requires the disclosure in a single prior art reference of each and every element of the claim under consideration, and each element must be arranged as in the claim. Bourke does not teach or suggest, as in independent claim 1, disabling interrupts on a computer system for entering a state of hibernation, preparing a first set of data for writing a first set of content of volatile memory to a disk, instructing a controller to write the first of data asynchronously to the disk, polling, in intermittent polling operations, a status register to determine when the write to the disk is

complete; and while between polling operations, preparing a second set of data for writing a second set of content of volatile memory to the disk.

For at least the above reasons, Bourke fails to meet the requirements for supporting a 35 U.S.C. §102(b) rejection of these claims, and applicants respectfully request reconsideration and withdrawal of the rejections of claim 1 based on Bourke. Similarly, Bourke does not teach or suggest the limitations present in claims 2-7 when analyzed in light of the use of disabling interrupts on a computer system for entering a state of hibernation and preparing a set of data for writing a set of content of volatile memory to a disk as described in independent claim 1. Therefore, claim 1 and the claims that depend thereon are patentable over the cited art.

Applicants also submit that the newly added claims 22-31 are also directed towards subject matter that is not taught in the prior art of record. For example, the new claim 22 generally recites: disabling interrupts on a computer system while resuming operation from hibernation; instructing a controller to asynchronously read data from a disk to an input buffer, the data representing contents of volatile memory previously stored on the disk from volatile memory; polling, in intermittent polling operations, a status register to determine when the read from the disk is complete; and while between polling operations, decompressing at least some data in the input buffer. The subject matter of these claims is not disclosed or suggested in the prior art of record. As such, the new claims 22-31 are each patentable over the prior art of record.

For at least these reasons, applicants submit that all the claims are patentable over the prior art of record. Reconsideration and withdrawal of the rejections in the Office action is respectfully requested and early allowance of this application is earnestly solicited.

CONCLUSION

In view of the foregoing remarks, it is respectfully submitted that claims 1-9, 12-15, and 22-31 are patentable over the prior art of record. Applicants also respectfully submit and that the application is in good and proper form for allowance. A favorable action on the part of the Examiner is earnestly solicited.

If in the opinion of the Examiner a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney at (425) 836-3030.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this Amendment and Petition for Extension of Time, along with Transmittal and Change of Correspondence Address are being deposited with the United States Postal Service on the date shown below with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Alexandria, VA 22313-1450

Date: March 12, 2004

Albert S. Michalik

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